Amendments to the Specification

Please replace the paragraph beginning on page 5, line 4, with the amended paragraph below.

TCAMs have the advantage of not requiring large and elaborate data structures, because they are specially designed for the purpose of lookup, but they have relatively high power usage, low speed and low density. Avoiding specialized memories leads to using other data structures, which in the known art are relatively large and therefore use multiple memory devices – either multiple ~~SRAM~~ DRAM (to achieve larger storage), or multiple ~~DRAM~~ SRAM chips (to achieve higher speed).

Please replace the paragraph beginning on page 5, line 18, with the amended paragraph below.

The invention provides a method and system for lookup of message header information that has the advantages of (1) the relative low scaling factor for power usage associated with the use of a random access memory such as SRAM, which has relatively constant power requirement relative to the amount of stored data, over that of associative memories such as TCAM, which has power requirement proportional to the amount of stored data, (2) the relative flexibility, associated with the use of a random access memory such as SRAM, over that of more specialized memories such as TCAM, (~~2~~3) the relative speed associated with on-chip memory over that of off-chip memory or associative memory. The invention includes methods and systems for lookup using pipelined on-chip memory to access any relatively compact and smaller data structures stored on-chip; one such relatively compact data structure is described in the incorporated disclosure, as referred to herein.

Please replace the paragraph beginning on page 8, line 19, with the amended paragraph below.

- U.S. Patent Application Serial No. ~~_____~~ 09/826,556, Express Mail Mailing No. EL734816260US, filed the same day in the name of the same inventors, attorney docket number 211.1002.01, titled "Compact Data Structures for Pipelined Message Forwarding Lookups."

Please replace the paragraph beginning on page 12, line 13, with the amended paragraph below.

The packet header information, having a total bit width of w, is coupled to the sequence of SRAM memories. Each stage n in the sequence includes an on-chip SRAM memory, an address lookup circuit, and a pipelined register, and spans dn bits of the total bit width. Thus, a first stage in the sequence includes a first on-chip SRAM memory 125, a first address lookup circuit 130, and a first pipeline register 135, and spans d1 bits of the total bit width; a second stage in the sequence includes a second on-chip SRAM memory 140, a second address lookup circuit 145, and a second pipeline register 150, and spans d2 bits of the total bit width; and so on until a final stage in the sequence includes a final on-chip SRAM memory and a final address lookup circuit ~~160~~ (except as described below, there is no particular requirement for a final pipeline register).

Please replace the paragraph beginning on page 22, line 11, with the amended paragraph below.

At a flow point 220, the method 200 is complete, and the final lookup result (if any) is coupled from the final stage best-match register ~~198~~ to the output port 104.